SUPPLEMENTAL AMENDMENTS TO THE CLAIMS

1.   (Currently Amended) A platform comprising:

a processor executing in one of a normal execution mode and an isolated execution mode;

a system memory accessible to the processor and including to store output data in an isolated area, an isolated output area; and a non-isolated area;

a memory controller hub (MCH) coupled to the system memory; and

a processor coupled to the MCH to generate a signal to the MCH, the signal indicating whether the output data is to be stored in the isolated output area or the non-isolated area, the signal generated by the processor to further cause the MCH to receive a bus transaction from a graphics device to enable access to the output data stored in the isolated output area in response to an indication of the signal that the output data is to be stored in the isolated output area of the system memory.

a graphics card coupled to the processor and accessible to different areas of the system memory according to access modes asserted by the graphics card.

2.   (Currently Amended) The platform of claim 1 wherein the bus transaction from the graphics card device comprises logics to handle output data from the isolated output area and the non-isolated area differently indicates an isolated transaction.

3.   (Currently Amended) The platform of claim 2 further comprising:wherein the a memory control hub (MCH) coupled between the system memory, the processor, and the graphics card device, the memory control hub to permit the graphics card device to access the isolated output area only when the graphics card device asserts an isolated access mode.

4.   (Currently Amended) The platform of claim 3 wherein the graphics card device comprises:

a direct memory access (DMA) controller and wherein local storage of the data in the graphics card from the isolated output area is not permitted.

5.   (Currently Amended) The platform of claim 3 wherein only the graphics card device is permitted to read the isolated output area.

6.   (Previously Presented) The platform of claim 1 further comprising:

an operating system (O/S) nub having a driver to write display data into the isolated output area when the processor is executing in the isolated execution mode.

7.   (Currently Amended) The platform of claim 3 further comprising:

a link between the graphics ~~card~~ device and the MCH having an isolated transaction type.

8.   (Original) The platform of claim 3 wherein the MCH only permits the O/S nub to write to the isolated output area.

9.   (Original) The platform of claim 7 wherein the link is a secure accelerated graphics port bus.

10.   (Currently Amended) The platform of claim 2 wherein the graphics ~~card~~ device comprises:

an isolated bit plane for the output data from the isolated output area; and

a non-isolated bit plane for the output data from the non-isolated output area.

11.   (Currently Amended) The platform of claim 10 wherein the graphics ~~card~~ device denies all external access to the isolated bit plane.

12.   (Currently Amended) A method comprising:

establishing an isolated execution environment having an isolated execution mode by a processor generating a signal indicating whether output data is to be stored in an isolated output area or a non-isolated area of a system memory, the signal generated by the processor further causing a memory controller hub (MCH) to receive a bus transaction from a graphics device to enable access to the output data stored in the isolated output area in response to an indication of the signal that the output data is to be stored in the isolated output area of the system memory~~providing hardware support for the isolated execution mode~~; and

preventing access to output data in ~~an~~ the isolated output area of ~~a~~ the system memory by any requester not operating in the isolated execution mode~~; and~~

~~handling the output data from the isolated output area and non-isolated area of the system memory differently at a graphics card that operates, and has different memory access privileges, in a normal execution mode and the isolated execution mode~~.

13.   (Canceled)

14.   (Currently Amended) The method of claim 12 further comprising:

issuing an isolated direct memory access (DMA) request for display data in the isolated

output area from the graphics ~~card~~device; and

refreshing the display based on the display data.

15.   (Previously Presented) The method of claim 12 wherein preventing comprises:

identifying if an isolated attribute is present in a request for access to the isolated output

area; and

denying the request if no isolated attribute is present.

16.   (Currently Amended) The method of claim 12 further comprising:

loading data from the isolated output area into a bit plane on the graphics ~~card~~device; and

denying all external access to the bit plane.

17.   (Previously Presented) The method of claim 16 further comprising:

defining a first window on an output display to present an image corresponding to the bit

plane; and

occluding all windows on the display but the first window.

18.   (Previously Presented) The method of claim 12 further comprising:

retrieving data from the isolated output area;

displaying an image corresponding to the data; and

occluding the image prior to a platform transitioning out of the isolated execution mode.

19.   (Currently Amended) ~~A platform~~An apparatus comprising:

a processor to generate a signal to a memory controller hub (MCH), the signal indicating

whether output data is to be stored in an isolated output area or a non-isolated area of a system

memory, the signal generated by the processor to further cause the MCH to receive a bus

transaction from a graphics device to enable access to the output data stored in the isolated output

area in response to an indication of the signal that the output data is to be stored in the isolated

output area of the system memory~~a processor executing in one of a normal execution mode and an isolated execution mode~~;

~~a direct memory access (DMA) controller to issue requests for access to an isolated output area of a system memory that includes the isolated output area and a non-isolated area;~~

~~a first interface coupled to the DMA controller to forward requests to a memory control hub (MCH); and~~

~~a graphics card coupled to the MCH to supply output data to an output device, the graphics card accessible to different areas of the system memory according to access modes asserted by the graphics card.~~

20.   (Currently Amended) The apparatus of claim 19 wherein the ~~first interface~~bus transaction is issued through a secure accelerated graphics port (AGP) ~~and the output device is a display~~.

21.   (Currently Amended) The apparatus of claim 19 wherein the bus transaction is issued by a direct memory access (DMA) controller of the graphics device, the DMA controller to attach ~~attaches~~ an isolated attribute to any isolated output area access request.

22.   (Currently Amended) The apparatus of claim 19 wherein the ~~graphic card comprises logics to handle the output data from the isolated output area and the non-isolated area differently~~signal generated by the processor has an isolated attribute to indicate execution in an isolated execution mode.